

WEST Search History

DATE: Saturday, October 30, 2004

<u>Hide?</u>	<u>Set Name</u>	<u>Query</u>	<u>Hit Count</u>
	<i>DB=PGPB,USPT; PLUR=NO; OP=ADJ</i>		
<input type="checkbox"/>	L44	bops.as. and shared and local	6
<input type="checkbox"/>	L43	bops.as. and global and local	3
<input type="checkbox"/>	L42	bops.as. and (global same local)	0
<input type="checkbox"/>	L41	6366999.pn.	1
<input type="checkbox"/>	L40	l35 not l38	38
<input type="checkbox"/>	L39	l35 not l38L38	503
<input type="checkbox"/>	L38	l35 not l37	465
<input type="checkbox"/>	L37	L36 not sun.as.	38
<input type="checkbox"/>	L36	vliw and L35	65
<input type="checkbox"/>	L35	global register\$1	503
<input type="checkbox"/>	L34	global register\$1 and L33	10
<input type="checkbox"/>	L33	712/24.ccls.	228
	<i>DB=USPT; PLUR=NO; OP=OR</i>		
<input type="checkbox"/>	L32	(synchroniz\$5 and vliw and 5574939.uref.)	10
	<i>DB=USPT; PLUR=NO; OP=ADJ</i>		
<input type="checkbox"/>	L31	synchroniz\$5 and L29	10
<input type="checkbox"/>	L30	synchriniz\$5 and L29	0
<input type="checkbox"/>	L29	vliw and L28	29
<input type="checkbox"/>	L28	5574939.uref.	54
	<i>DB=EPAB,JPAB,DWPI,TDBD; PLUR=NO; OP=ADJ</i>		
<input type="checkbox"/>	L27	5574939.uref.	0
<input type="checkbox"/>	L26	clustered vliw	2
<input type="checkbox"/>	L25	multiple vliw cores	0
<input type="checkbox"/>	L24	multiple vliw cores	0
<input type="checkbox"/>	L23	vliw and L22	12
<input type="checkbox"/>	L22	multiprocessor or multi-processor or (multiple processors)	12450
	<i>DB=PGPB,USPT; PLUR=NO; OP=ADJ</i>		
<input type="checkbox"/>	L21	L6 with vliw	50
<input type="checkbox"/>	L20	clustered vliw	5
<input type="checkbox"/>	L19	variable issue width	10
<input type="checkbox"/>	L18	synchroniz\$5 same L17	4

<input type="checkbox"/>	L17	vliw processors	299
<input type="checkbox"/>	L16	multiple vliw cores	2
<input type="checkbox"/>	L15	multiple vliw processors	0
<input type="checkbox"/>	L14	multiple vliw pipelines	0
<input type="checkbox"/>	L13	vliw same L12	25
<input type="checkbox"/>	L12	multiple pipelines	419
<input type="checkbox"/>	L11	vliw and L10	5
<input type="checkbox"/>	L10	5459798.uref.	22
<input type="checkbox"/>	L9	vliw same L8	4
<input type="checkbox"/>	L8	L6 with chip	1040
<input type="checkbox"/>	L7	L6 adj chip	56
<input type="checkbox"/>	L6	multiprocessor or multi-processor or (multiple processors)	26036
<input type="checkbox"/>	L5	vliw and L4	6
<input type="checkbox"/>	L4	pipeline paths	24
<input type="checkbox"/>	L3	L1 same L2	12
<input type="checkbox"/>	L2	"two register files"	172
<input type="checkbox"/>	L1	"single register file"	148

END OF SEARCH HISTORY